PATMOS
VARI 2014




Conference Program

Palma de Mallorca
September 29 – October 1, 2014

Welcome

Welcome to PATMOS/VARI 2014 and to the University of Balearic Islands.

The traditional scope of the PATMOS conference series has mainly been about and around the design of circuits and architectures optimized for highest performance at lowest power consumption. But meanwhile, power-efficiency has become extremely important for many more areas spreading far beyond this traditional R&D niche.

VARI is devoted to explore the variability in CMOS process, as well as its sensitivity to environmental variations, which have become a major challenge to scaling and integration. This leads to major changes in the way that future integrated circuits and systems are designed.

Both conferences addresses complementary topics and, therefore, we hope that its collocation will be appreciated by the attendants to both conferences and will generate synergies among the respective programs. Our objective is to create a forum where industry and academia meet, a forum to discuss and investigate the current and upcoming generations of integrated circuits and systems. We encourage you to take advantage of this opportunity to interact with colleagues and to share your knowledge and insights.

We would like to thank the Steering Committees of both conferences and the volunteers who have made this event happen. Thanks also to the Program Committees for his work in the review process.

We hope you enjoy the conference and your time in Palma de Mallorca

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VARI 2014

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Practical Information

Full program

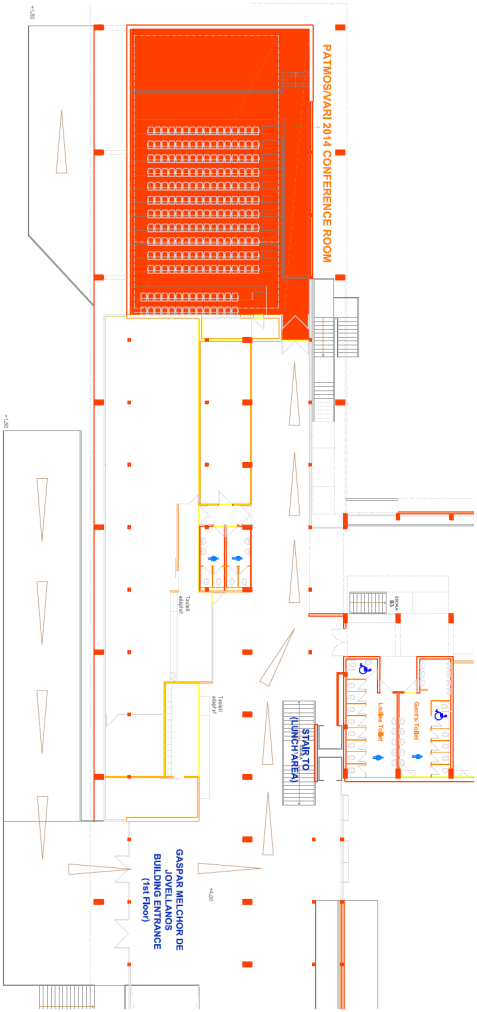
This is the short program containing all relevant information in a compact manner. You can find the full program that also includes the full abstracts on the USB stick in your conference folder.

Conference venue

The PATMOS/VARI 2014 conference takes place in Palma de Mallorca at Campus of the University of Balearic Islands. All sessions will take place in the “Sala de Actos” of Gaspar Melchor de Jovellanos Building.

UIB CAMPUS

GASPAR MELCHOR DE JOVELLANOS BUILDING



Coffee breaks and lunches will be held in the Cafeteria (building ground floor, downstairs) of the same building. All directions will be signposted.

Registration Desk

The registration and information desk is open during the get-together as well as during the coffee breaks and the sessions. You can find the desk right at the main entry of the Gaspar Melchor de Jovellanos Building.

Guidelines for Speakers and Sessions Chairs

The session room will be equipped with a laptop and a computer projector. Please be on time for your session and check in with your session chair. A volunteer or organizer will be available to set up your presentation and help you with any issue you might encounter. Presentations should emphasize the key issues and conclusions. Each speaker has in total 25 minutes for presentation and discussion, we propose to use at most 20 minutes for the presentation.

The chair coordinates the session. He/she introduces each presentation, informs the speaker when the time is running short and leads the discussion.

WIFI network guide

1. Wifi Network guide for EDUROAM users:

Our university participates in the eduroam initiative. Attendants coming from an institution that belongs to the Eduroam program can get connected to the "eduroam" wireless network. In order to get connected to this network, the credentials (username/password) served by the foreign institution must be used.

2. General WiFi network guide

A. Connect to the WiFi (or SSID) "uib_(key=password2014)" network.
B. Introduce the key "password2014"
C. Activate the dynamic IP configuration (DHCP). It's very usual to have dynamic configuration set on the wireless interfaces. Typically it won't be necessary to perform this step.
D. Open a web browser and try to access a website. Insert the following credentials in the web page that will appear:

Username: patmos
Password: jovellanos2014

Note: The connection to the "uib_(key=password2014)" and "eduroam" wireless network can be established from anywhere in the UIB campus (to know the wireless network availability a map can be found at http://www.cti.uib.es/eduroam).
Anyone using the account must be somehow related to the PATMOS-VARI 2014 meeting.

MONDAY, Sept. 29th 2014		TUESDAY, Sept. 30th 2014		WEDNESDAY, Oct. 1st 2014	
8:00 9:00	Registration				
9:00 9:20	Wellcome and Opening				
9:20 10:20	Keynote: Arlindo Oliveira. **CAD Techniques in Computational Biology**	8:30 10:35	VARI Session 1 Variability in Memories	8:30 10:35	PATMOS Session 7 System Level Power Management
10:20 10:45	Break and Posters	10:35 11:00	Break and Posters	10:35 11:00	Break and Posters
10:45 12:00	PATMOS Session 1 Modeling, Simulation and Circuit Optimization I	11:00 12:00	Keynote: Massimo Alioto. **Designing (relatively) unreliable systems with (highly) unreliable components**	11:00 12:00	Keynote: J. N. Burghartz. **Ultra-thin Chips - a New Paradigm in SiliconTechnology**
12:00 13:15	PATMOS Session 2 Power estimation	12:00 13:15	PATMOS Session 5 Emerging Technologies	12:00 13:15	PATMOS Session 8 Low Power Techniques
13:15 14:30	Lunch	13:15 14:30	Lunch	13:15 14:30	Lunch
14:30 16:10	PATMOS Session 3 Yield, Robustness and Power Efficiency	14:30 16:10	VARI Session 2 Variability at Technology and Device Levels	14:30 16:10	VARI Session 3 Variability at Circuit Level
16:10 16:30	Coffee Break	16:10 16:30	Coffee Break	16:10 16:30	Coffee Break
16:30 18:10	PATMOS Session 4 Power and Timing Efficiency	16:30 17:45	PATMOS Session 6 Modeling, Simulation and Circuit Optimization II	16:30 18:10	PATMOS Session 9 Power Estimation and Optimization
				18:10	Closing Remarks
		19:30	Social Event and Gala Dinner		

Conference Schedule

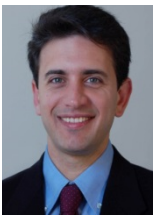
Keynote speakers

Monday, 09:20-10:20

Arlindo Oliveira: CAD Techniques in Computational Biology

Abstract: During the last four decades, many algorithms have been developed in the area of Computer Aided Design (CAD) with the objective of supporting circuit designers in the phases of circuit design, verification and test. Coupled with the advances in VLSI technology, these algorithms are at the core of our ability to design circuits with many millions of elements. Recently, with the development of high throughput techniques for biological data and the improved knowledge of biological processes that they supported, it has been possible to design complex models for biological systems that can use many of the algorithms, formalisms and approaches that have been developed by the CAD community. Up to now, simulation and model verification techniques are the most popular tools borrowed by biologists from the CAD community. With the advent of synthetic biology, and the need for tools that support the design of complex systems, other techniques that were created by the CAD community are likely to find their place amongst the methods used by biologists and bioinformaticians in their quest for tools that help them design, simulate and validate models for new and existing biological systems.

Thuesday, 11:00-12:00



Massimo Alioto: Designing (relatively) unreliable systems with (highly) unreliable components

Abstract: Almost ten years after the breed of papers and keynotes speeches on the design of reliable systems with unreliable components, the design challenges posed by variations are harder than ever. To reduce the large energy cost of computational correctness due to variations, the VLSI community is now exploring ways to embrace imperfect computation, instead of over-constraining circuits/systems to hide the natural imperfection of hardware. However, the field of “approximate computing” is still in its infancy, and most of the related work is highly fragmented and not really focused on the real challenges ahead of us.

In this talk, a vision on how mainstream processing platforms can incorporate imperfect computation will be presented. In particular, we will introduce a unitary framework for systems that dynamically trade energy and "quality of computation" off, depending on the application and the user's requirements. To address one of the key related challenges, fresh concepts to preserve the economy of scale offered by todays' design approaches will be discussed. In particular, ideas will be discussed on how to incorporate dynamic energy-quality management in general-purpose systems, designed with existing EDA tools, and programmed with existing software programming models (or so). Unsurprisingly, variation-aware and across-boundary design are two key concepts that represent a common thread for this keynote speech. To open up a broader perspective, variation-aware circuit techniques and design strategies will be discussed to enable dynamic and wide energy-quality adjustment in sub-32nm technologies, from error-tolerant to error-free. Appropriate abstractions, architectures and control schemes will be discussed to propagate such capability at all levels.

As main conclusion, imperfection and variations can actually be used to enrich the traditional perfect computational paradigm, rather than disrupt it. But this requires a much more diffused (and profound) awareness of variations in both the hardware and the software community.

Wednesday, 11:00-12:00

J. N. Burghartz: Ultra-thin Chips - a New Paradigm in SiliconTechnology

Abstract: In contrast to conventional thick silicon chips ultra-thin chips will be the basis for new applications, such as 3D integrated circuits (3D-ICs) and plastic electronics. This talk will introduce and compare two generically different process technologies that can be exploited for the fabrication of ICs on extremely thin chips. Furthermore, several application results and demonstrations will be presented and discussed based on material that has been presented at the recent IEDM and ISSCC conferences.

Program

Monday, 09:20-10:20
PATMOS Keynote

Arlindo Oliveira. **CAD Techniques in Computational Biology**

Monday, 10:20-10:45
Break and Poster Session (PATMOS)

Low-Power Design Methodology for CML and ECL Circuits
Oliver Schrape, Markus Appel, Frank Winkler, Milos Krstic.

DOE based high performance gate-level pipelines
Juan Núñez, Héctor J. Quintero and María J. Avedillo.

Power-Efficient Power-Management Logic
Dominik Macko, Katarína Jelemenská and Pavel Čičák.

GALS Design of ECC against Side Channel Attacks - A Comparative Study
Xin Fan, Steffen Peter, Milos Krstic

VPPET: Virtual Platform Power and Energy Estimation Tool for Heterogeneous MPSoC based FPGA Platforms
Santhosh Kumar Rethinagiri, Oscar Palomar, Javier Arias, Adrian Cristal, Osman Unsal.

Low-cost Hardware Implementation of Reservoir Computers
Miquel L. Alomar, Vincent Canals, Victor Martinez-Moll and Josep L Rossello.

Monday, 10:45-12:00
PATMOS Session 1: Modeling, Simulation and Circuit Optimization I

Session chair: Spyridon Nikolaidis

10:45 Convex Optimization of Resource Allocation in Asymmetric and Heterogeneous SoC
Amir Morad, Leonid Yavits, Ran Ginosar.

11:10 Equivalence of Clock Gating and Synchronization with Applicability to GALS Communication
Robert Najvirt and Andreas Steininger.

11:35 Fast Modeling Technique for Nano Scale CMOS Inverter and Propagation Delay Estimation
Abdoul Rjoub and Areej Ahmad.

Monday, 12:00-13:15
PATMOS Session 2: Power Estimation

Session chair: Ricardo Reis

12:00 Fast and Accurate Solution for Power Estimation and DPA Countermeasure Design
Daniel Vidal and Mário Côrtes.

12:25 Formal Description of an Approach for Power Consumption Estimation of Embedded Systems
Dmitriy Shorin and Armin Zimmermann.

12:50 A Methodology for Scaling Power Dissipation Values Between Different FPGAs
Axel Reimer and Wolfgang Nebel.

Monday, 14:30-16:10
PATMOS Session 3: Yield, Robustness and Power Efficiency

Session chair: Alex Yakovlev

14:30 Parametric Yield Optimization Using Leakage-Yield-Driven Floorplanning
Yang Xu, Bo Wang and Jürgen Teich.

14:55 Experimental Analysis of Flip-Flops Minimum Operating Voltage in 28nm FDSOI Power and Timing Efficiency and the Impact of Back Bias and Temperature
Sébastien Bernard, Marc Belleville, Alexandre Valentian, Jean-Didier Legat, David Bol.

15:20 Power Efficient Digital IC Design for a Medical Application with High Reliability Requirements
Nasim Pour Aryan, Nils Heidmann, Martin Wirnshofer, Nico Hellwege, Jonas Pistor, Dagmar Peters-Drolshagen, Georg Georgakos, Steffen Paul, Doris Schmitt-Landsiedel.

15:45 A Power-Efficient FPGA-Based Self-Adaptive Software Defined Radio
Chris Dobson, Kurt Rooks and Peter Athanas.

Monday, 16:30-18:35
PATMOS Session 4: Power and Timing Efficiency

Session chair: Vasily Moshnyaga

16:30 Efficient dense and sparse matrix multiplication on GP-SIMD
Amir Morad, Leonid Yavits and Ran Ginosar.

16:55 Impact of Task Offloading on Efficiency of Wireless Face Recognition
Nanako Sumi, Akiya Baba and Vasily Moshnyaga.

17:20 Fast Energy Evaluation of Embedded Applications for Many-core Systems
Felipe Da Rosa, Luciano Ost, Thiago Raupp, Fernando Moraes, Ricardo Reis.

17:45 A Global Perspective on Energy Conservation in Large Data Networks
Lisa Durbeck, Peter Athanas.

Tuesday, 8:30-10:35
VARI Session 1: Variability in Memories

Session chair: Marisa López-Vallejo

8:30 Reliability Challenges in Design of Memristive Memories
Peyman Pouyan, Esteve Amat, Antonio Rubio.

8:55 Characterization of Random Telegraph Noise and its impact on reliability of SRAM sense amplifiers
Javier Martin Martinez, Javier Diaz, Rosana Rodríguez, Montserrat Nafria, Xavier Aymerich, Elisenda Roca, Francisco Vidal Fernandez, Antonio Rubio.

9:20 Variability impact on on-chip memory data paths
Esteve Amat, Antonio Calomarde, Ramon Canal and Antonio Rubio.

9:45 SRAM Write Margin Cell Estimation using Word- line Modulation and read/write operations
Bartomeu Alorda, Cristian Carmona, Gabriel Torrens

10:10 Comparative Evaluation of Tunnel-FET Ultra-Low Voltage SRAMs and Impact of Variations
Massimo Alioto, David Esseni.

Tuesday, 10:35-11:00
Break and Poster Session (VARI)

MIDAS: Model for IP-inclusive DFM Assessment of System Manufacturability
Kasyab Parmesh Subramaniyan and Per Larsson-Edefors.

Analysis and Comparison of Variations in Double Edge Triggered Flip-Flops
Massimo Alioto, Elio Consoli, Gaetano Palumbo.

A Tool for the Automatic Analysis of Single Events Effects on Electronic Circuits
Fernando García-Redondo, Pablo Royer, Javier Agustín Sáenz and Marisa Lopez-Vallejo.

Tuesday, 11:00-12:00
VARI Keynote

Massimo Alioto. **Designing (Relatively) Unreliable Systems with (Highly) Unreliable Components**

Tuesday, 12:00-13:15
PATMOS Session 5: Emerging Technologies

Session chair: Delong Shang

12:00 Evaluating the Impact of Environment and Physical Variability on the Current of 20nm FinFET Devices
Alexandra L. Zimpeck, Cristina Meinhardt, Ricardo A. L. Reis

12:25 Write Scheme for Multiple Complementary Resistive Switch (CRS) Cells
Adedotun Adeyemo, Abusaleh Jabir, Jimson Mathew, Dhiraj Pradhan.

12:50 A Scalable Physical Model for Nano-Electro-Mechanical Relays
Haider Alrudainy, Andrey Mokhov and Alex Yakovlev.

Tuesday, 14:30-16:10
VARI Session 2: Variability at Technology and Device Levels

Session chair: Nadine Azemard

14:30 Variability characterisation of nanoscale Si and InGaAs FinFETs at subthreshold
Guillermo Indalecio, Natalia Seoane, Manuel Aldegunde, Karol Kalna, Antonio Jesus Garcia-Loureiro.

14:55 TCAD simulation of interface traps related variability in bulk decananometer MOSFETs
Vikas Velayudhan, Javier Martin, Montserrat Nafria Maqueda, Rosana Rodriguez, Marc Porti, Francisco Gamiz, Cristina Medina, Xavier Aymerich.

15:20 Four-Injector Variability Modeling of FinFET Predictive Technology Models
Pablo Royer, Marisa Lopez-Vallejo, Fernando García Redondo, Carlos A. López Barrio.

15:45 Circuit Optimization using Device Layout Motifs
Yang Xiao, Martin Trefzer, Scott Roy, James Walker, Simon Bale, Andy Tyrrell.

Tuesday, 16:30-17:45
PATMOS Session 6: Modeling, Simulation and Circuit Optimization II

Session chair: Antonio Acosta

16:30 Gate Leakage Current Accurate Models for Nanoscale MOSFET Transistors
Abdoul Rjoub, Nedal Taradeh and Mamoun Mistarihi.

16:55 An Analytical Model for the CMOS Inverter
Panagiotis Chaourani, Ioannis Messaris, Nikolaos Fasarakis, Maria Ntogramatzi, Sotirios Goudos and Spyridon Nikolaidis.

17:20 A Framework for Efficient Evaluation and Comparison of EES Models
Sara Vinco, Alessandro Sassone, Davide Lasorsa, Enrico Macii and Massimo Poncino.

Tuesday, 19:30
Social Event and Gala Dinner

Wednesday, 8:30-10:35
PATMOS Session 7: System Level Power Management

Session chair: Miquel Roca

8:30 A Lightweight-System-Level Power and Area Estimation Methodology for Application Specific Instruction Set Processors
Syed Abbas Ali Shah, Jan Wagner, Thomas Schuster and Mladen Berekovic.

8:55 Application-aware Scaling Governor for Wearable Devices
Jae Min Kim, Minyong Kim and Sung Woo Chung.

9:20 Advanced SoC Virtual Prototyping for System-Level Power Planning And Validation
Fabian Mischkalla, Wolfgang Mueller.

9:45 End-to-End Power Estimation for Heterogeneous Cellular LTE SoCs in Early Design Phases
Bo Wang, Yang Xu, Ralph Hasholzner, Rafael Rosales, Michael Glaß and Jürgen Teich.

10:10 Energy management of highly dynamic server workloads in an heterogeneous data center
Efraim Rotem, Uri Weiser, Avi Mendelson, Ahmad Yasin. Ran Ginosar.

Wednesday, 10:35-11:00
Break and Poster Session (PATMOS)

Energy consumption savings in ZigBee-based WSN adjusting power transmission at application layer
Cristian Carmona, Miquel Angel Ribot and Bartomeu Alorda.

A Methodology to Evaluate Energy Saving Techniques in Data Buses Transmission
J. Sanchez, J.M. Gil-Garcia, J.A. Sainz, Eugeni Isern and Miquel Roca.

A unique network EDA tool to create optimized ad hoc binary to residue number system converters
Giannis Petrousov and Minas Dasygenis.

A distributed VHDL compiler and simulator accessible from the web
Minas Dasygenis.

Optimization on Cell-library Design for Digital Application Specific Printed Electronics Circuits
Jody Matos, Manuel Llamas, Mohammad Mashayekhi, Jordi Carrabina, André Reis.

Wednesday, 11:00-12:00

PATMOS Keynote 2

Joachim N. Burghartz. **Ultra-thin Chips - a New Paradigm in Silicon Technology**

Wednesday, 12:00-13:15
PATMOS Session 8: Low Power Techniques

Session chair: Sergio Bampi

12:00 Power-Efficient Turbo-Decoder Design based on Algorithm-Specific Power Domain Partitioning
Christoph Roth, Christian Benkeser, Qiuting Huang.

12:25 Design and Test of a Low-Power 90nm Xor/Xnor Gate for Cryptographic Applications
Erica Tena, Javier Castro, Antonio Acosta.

12:50 Robust Sub-Powered Asynchronous Logic
Jiaoyan Chen, Emanuel Popovici, Arnaud Tisserand, Sorin Cotofana.

Wednesday, 14:30 - 16:10
VARI Session 3: Variability at Circuit Level

Session chair: Manuel Bellido

14:30 All-digital self-adaptive PVTA variation aware clock generation system for DFS
Jordi Pérez Puigdemont, Antonio Calomarde and Francesc Moll.

14:55 Adaptive Sized Quasi-Monte Carlo Based Yield Aware Analog Circuit Optimization Tool
Engin Afacan, Gönenç Berkol, Ali Emre Pusane, Günhan Dündar and Faik Başkaya.

15:20 Fractional Phase Divider PLL Phase Noise and Spurious modeling
Alexandre Fonseca, Emeric De Foucauld, Philippe Lorenzini, Gilles Jacquemod.

15:45 Comparison of Bulk Built-In Current Sensors in terms of Transient-Fault Detection Sensitivity
Rodrigo Possamai Bastos, Jean-Max Dutertre, Frank Sill Torres.

Wednesday, 16:30 - 18:10
PATMOS Session 9: Power Estimation and Optimization

Session chair: Eugeni Isern

16:30 Estimating Power Consumption of Multiple Modular Redundant Designs in SRAM-based FPGAs for High Dependable Applications
Jimmy Tarrillo and Fernanda L. Kastensmidt.

16:55 Hardware-assisted Power Estimation for Design-stage Processors using FPGA Emulation
Sebastian Hesselbarth, Tim Baumgart and Holger Blume.

17:20 Rate-Distortion and Energy Performance of HEVC Video Encoders
Eduarda Monteiro, Mateus Grellert, Bruno Zatt, Sergio Bampi.

17:45 Tunning Software-based Fault-tolerance Techniques for Power Optimization
Eduardo Chielle, Fernanda Lima Kastensmid, Sergio Cuenca-Asensi

Wednesday, 18:10
Closing Remarks

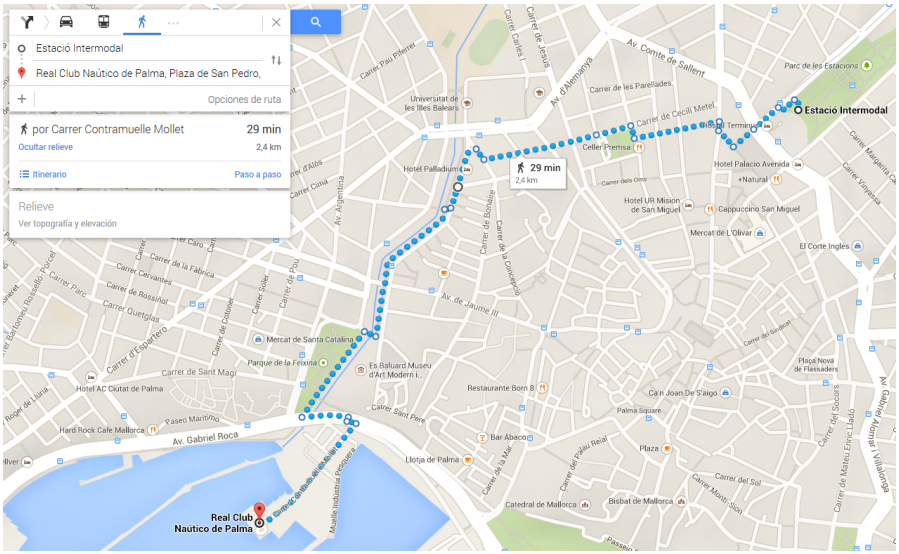
Social program

Tuesday, September 30 (19:30). City tour Palma

We will follow a English-speaking guided tour to the most stunning spots in the city. The walking tour takes one hour. Departure is in Plaza España at 19.30. In front of the Metro station "Estación Intermodal" (see the map below). The tour will end at the entrance of the "El Nautico" restaurant.

Tuesday, September 30 (20:30). Gala dinner

The gala dinner will be held at Restaurant “El Náutico”, a very famous restaurant in Palma, which is located in the Real Club Náutico de Palma. It has fabulous views of the Yacht Club, the bay of Palma and the Paseo Maritimo. (see the map below).



List of Participants



Universitat de les Illes Balears

#SOM UIB

A campus spanning four islands
The main Campus in Palma de Mallorca
Off-campus Centre of Ibiza and Formentera
Off-campus Centre of Menorca

Academic Offer
Bachelor's degrees : 36
Official masters: 33
Doctoral Programs : 26
Postgraduate courses: 77

University community
Teaching and Research Staff: 1743
Administration and Services Staff: 527
Students: 18.182

Rankings *
· Best national university in the quality of research
· Second best university in Europe on tourism research
· Third national university in research production
· Fourth national university in the quality of teaching

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