DATE PhD Forum 2016

The DATE PhD forum is part of the DATE Conference and hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). It offers the opportunity for PhD students to present their thesis work to a broad audience in the design, automation and test community from academia and industry. During the presentation at the DATE Conference, it helps students to establish contacts. Representatives from industry and academia get a glance of state-of-the-art research in design, automation and test. The review process resulted in the selection of the PhD students listed below. We thank EDAA, ACM SIGDA, CEDA and DATE for making this forum possible.

Rolf Drechsler, University of Bremen/DFKI GmbH, DE (Chair, DATE PhD Forum 2016)

PhD Forum Committee
Valeria Bertacco, University of Michigan, US
Davide Bertozzi, University of Ferrara, IT
Anupam Chattopadhyay, Nanyang Technological University, SG
Mingsong Chen, East China Normal University, CN
Yiran Chen, University of Pittsburgh, US
Giorgio Di Natale, LIRMM, FR
Nikil Dutt, UC Irvine, US
Franco Fummi, Universita' di Verona, IT
Shiyan Hu, Michigan Technological University, US
Younghyun Kim, Purdue University, US
Bing Li, Technische Universität München (TUM), DE
Martha Johanna Sepulveda Florez, Technische Universität München (TUM), DE
Sander Stuijk, Eindhoven University of Technology, NL
Daniel Tille, Infineon Technologies, DE
Miroslav N. Velev, Aries Design Automation, US
Natarajan Viswanathan, IBM Corporation, US
Robert Wille, Johannes Kepler University, AT
Pingqiang Zhou, Shanghai Tech University, CN

Admitted Presentations

1. **A Method for Power Abstraction and Simulation of Hardware Components at System Level**
   Daniel Lorenz, OFFIS, DE

2. **Auto-tuning Techniques for Compiler Optimization**
   Amir Hossein Ashouri, Politecnico Di Milano, IT

3. **System-Level Design of Embedded Systems for Reliability**
   Hananeh Aliee, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

4. **Analyzing Systems for Correct Implementation of Robustness**
   Niels Thole, University of Bremen, DE

5. **Novel EDA techniques for Printed Electronics Circuits**
   Manuel Llamas, UAB, ES

6. **Proactive Power and Thermal Aware Optimizations for Energy-Efficient Cloud Computing**
   Patricia Arroba, Universidad Politecnica de Madrid, ES

7. **Research on VLSI architecture for Intra prediciton in H.265 for 8K UHDTV video decoder**
   Jianbin Zhou, Waseda University, JP

8. **Enabling Caches in Probabilistic Timing Analysis**
   Leonidas Kosmidis, Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES

9. **Resilient Design for Three-Dimensional Integrated Circuits**
   Shengcheng Wang, Karlsruhe Institute of Technology, DE

10. **Low-Power High-Performance High-Reliable Spintronic Design**
    Rajendra Bishnoi, Karlsruhe Institute of Technology, DE

11. **Automatic Reconfigurable Platforms Design**
    Carlo Sau, University of Cagliari, IT

12. **Robust Image Processing Hardware Acceleration on Reconfigurable Devices for Critical Applications**
    Pascal Trotta, Politecnico di Torino, IT

13. **Novel Reliability Estimation Techniques for Nano-scale Circuits Affected by Noise, Process Variations and Aging**
    Usman Khalid, Sapienza University of Rome, IT

14. **Analysis, Design, and Optimization of Embedded Control Systems**
    Amir Aminifar, Linköping University, SE

15. **Hardware-enhanced run-time Management for Many-Core Processors**
    Daniel Gregorek, University of Bremen, DE

16. **Design and Formal Analysis of Run-DMC, A Dynamically-Scheduled Real-Time Memory Controller**
    Yonghui Li, Eindhoven University of Technology, NL

17. **Exploiting Body Biasing in Dynamically Reconfigurable Processors**
    Johannes Maximilian Kühn, Keio University/Eberhard Karls Universität Tübingen, JP

18. **Optimization and Complexity Analysis of Quantum Circuits**
    Abdessaied Nabila, University of Bremen, DE

19. **Generating Optimal Functional Coverages in Digital Systems**
    Alfonso Martinez, Computer Research Center (CIC-IPN), MX

20. **Holistic Actor-Oriented Modeling of Embedded Systems for ESL Power Consumption Evaluation**
    Rafael Rosales, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

21. **Uncertainty Quantification of Integrated Circuits and Microelectromechanical Systems**
    Zheng Zhang, MIT and Argonne National Labs, US

22. **A Homogeneous Platform-Based Design Approach for the Design of Heterogeneous Systems**
    Michele Lora, University of Verona, IT

23. **Modeling and Mitigation of Parametric Time-Dependent Variability in Digital Systems**
    Dimitrios Rodopoulos, ICCS/NTUA, GR

24. **Highly Automated Formal Verification of Arithmetic Circuits**
    Amr Sayed Ahmed, University of Bremen, 28359 Bremen, Germany, DE

25. **A Platform for High-Performance and Power-Aware Network Processing on GPUs**
    Federico Busato, University of Verona, IT

26. **FPGA Mapping Considering Aging and Process Variation**
    Mohammad Ebrahimi, University of Tehran, IR

27. **Circuit-Level Optimizations for Cryptography**
    Vladimir Rozic, ESAT/COSIC and iMinds, KU Leuven, BE

28. **Design and Scheduling of Real-Time Embedded Systems**
    Zaid Al-bayati, McGill University, CA