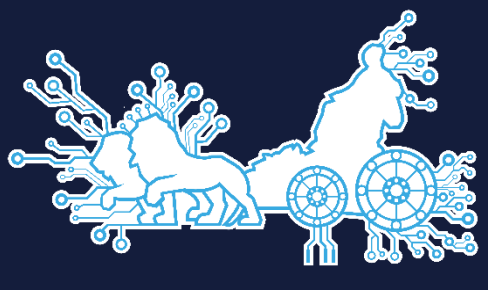
XXIX Conference on
Design of Circuits and Integrated Systems

DCIS 2014



Conference Technical Program

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Program at a Glance

	Wednesday, November 26th			
8:00 - 9:00	Registration			
9:00 - 9:30	Conference Opening Session			
9:30 - 10:30	Plenary Session 1 Putting Computing on a Strict Diet With Energy-Proportionality (Alex Yakovlev)			
10:30 - 11:30	1A. Analog & RF Design	1B. Modeling & Simulation	1C. SS Teaching and Learning in the DCIS I	
11:30 - 12:00	Coffee Break			
12:00 - 13:20	2A. SS - Teaching and Learning in the DCIS II	2B. Low Power / Low Voltage Analog Design	2C. FPGAs	2D. Failure Analysis
13:20 - 15:00	Lunch Break			
15:00 - 16:20	3A. Image and Graphic Processing	3B. Analog Design	3C. Integrated Sensors and Applications	3D. Reliability
16:20 - 17:00	Coffee Break			
17:00 - 18:20	Tutorial 1	Tutorial 2	Tutorial 3	
19:00 - 21:00	Welcome Cocktail			

	Thursday, November 27th			
9:00 - 10:00	Plenary Session 2 From Evolvable Hardware to Approximate Computing (Lukáš Sekanina)			
10:00 - 11:20	Tutorial 4	Tutorial 5	Tutorial 6	
11:20 - 12:00	Coffee Break			
12:00 - 13:20	4A. SS Power Management & Ultra-Low-Power Circuits	4B. Single Event Transient and Upset	4C. Communications	4D. Digital Design
13:20 - 15:00	Lunch Break			
15:00 - 16:20	5A. Organic Electronics	5B. Applications I	5C. Architectures	5D. Device Technology
16:20 - 18:00	Panel Quo Vadis Zero Power Design: A System-Driven Debate (Antonio Rubio)			Tutorial 7
18:30 - 23:00	Social Event Conference Dinner			

	Friday, November 28th		
9:40 - 11:00	6A. Applications II	6B. Modeling	6C. Digital Signal Processing
11:00 - 11:40	Coffee Break		
11:40 - 13:00	7A. Analog III	7B. Biomedical Electronics	7C. Built-In Self-Test
13:00 - 13:30	Conference Closing Session		
13:30 - 15:00	Lunch Break		

Sessions A will be held at Room C.

Sessions B will be held at Room D.

Sessions C will be held at Room María Fernández del Amo.

Sessions D will be held at Room Salón de Actos.

Conference Opening and Closing Sessions, Plenary Sessions 1 and 2 and the Panel Session will be held at Room Salón de Actos.

WEDNESDAY 26TH

Conference Opening Session. 9:00-9:30 (Room Salón de Actos)

Plenary Session 1. 9:30-10:30 (Room Salón de Actos)

Prof. Alex Yakovlev, Newcastle University, UK

Professor Alex Yakovlev was a Dream Fellow of the prestigious UK Engineering and Physical Sciences Research Council in 2011-12 to investigate different aspects of energy-modulated computing. He received DSc from Newcastle University in 2006, and PhD from St. Petersburg Electrical Engineering Institute in 1982. Since 1991 he has been at Newcastle University, where he is currently leading the microSystems research group at the School of Electrical and Electronic Engineering. His main interests and publications are in the field of modelling and design of asynchronous, concurrent, real-time and real-power systems, and autonomous systems for survival. For more information: http://async.org.uk and http://www.ncl.ac.uk/eee/staff/profile/alex.yakovlev

Putting Computing on a Strict Diet with Energy-Proportionality

Abstract: The traditional approach to designing power-aware computing systems is based on optimizing the energy consumption of a system for a given set of operating conditions, such as power supply, temperature range etc., and for requirements on performance, such as throughput and reliability.

For systems that are significantly power-constrained, such as autonomous or implanted electronic devices, energy usage is an essential factor in the system's requirements, and not just an optimization criterion. In this type of systems, the behavioral profile of the system is determined by both power delivery and information flow, often intertwined. In the extreme case, even the information can enter the system in the form of energy. For example, consider a system of sensors monitoring the energetic field (mechanical, thermal or photovoltaic) of some area. Here, the energy of each point in the field is both the driver of the sensor's activity and the source of data. Design of such systems must be holistic in the sense that both information and energy paths have to be considered in close interaction. Making only part (in time or in space) of the system's functionality energy-efficient, for example, when its computational load is guaranteed a well-regulated power source, while the energetic cost of voltage regulation is ignored, would be wrong. At present, there is no sound theory and methodology of designing systems that are energy-modulated or what we may call here "real-power systems". Systems are not sufficiently power-proportional, i.e. their functionality, e.g. computation activity, is not proportional to energy consumption. One of the stumbling blocks is in the domain of timing, which is usually determined by a clock generator, whose operation is not directly related to the energy source.

Self-timed or asynchronous systems design offers ways to building systems that are both robust and efficient for the above-mentioned regimes of work. This talk will look at a number of systematic techniques for designing systems with more predictable energy consumption from the transistor level upwards. It will also illustrate this potential of self-timed circuits with

a number of examples, including speed-independent SRAM, reference-free voltage sensor, self-timed microprocessor, and voltage regulation for sporadic and intermittent power supply.

Session 1A. Analog & RF Test. 10:30-11:30 (Room C)

Session Chairs: José Machado, Adoración Rueda

Quality Metrics for Mixed-Signal Indirect Testing
Alvaro Gomez-Pau, Luz Balado and Joan Figueras *(Universidad Politécnica de Catalunya)*

Fault List Compression for Efficient Analogue and Mixed-Signal Production Test Preparation
Nuno Guerreiro *(INESC-ID / IST)*, Marcelino Santos *(SiliconGate / INESC-ID / IST)* and J. Paulo Teixeira *(INESC-ID / IST)*

A SEU noise model for a spread spectrum wireless communication system
Patricio López González, Vicente Baena Lecuyer, Hipólito Guzmán Miranda, Javier Barrientos Rojas and Miguel Ángel Aguirre Echánove *(Universidad de Sevilla)*

Session 1B. Modeling & Simulation. 10:30-11:30 (Room D)

Session Chairs: Ramón González, Jaume Segura

Fast hardware-in-the-loop verification platform: a case study for convolutional decoders
Aritz Alonso and Andoni Irizar *(Centro de Estudios e Investigaciones Técnicas)*

Static Gate Power Consumption Model based on Power Contributors
Ioannis Messaris, Nikolaos Karagiorgos, Spiros Nikolaidis and Panagiotis Chaourani *(Aristotle University of Thessaloniki)*

High-Performance Digital Subthreshold Logic
Daniel Orradre, Antonio Lopez-Martin, M. Pilar Garde, Jaime Ramirez-Angulo and Ramon G. Carvajal *(Universidad Pública de Navarra)*

Session 1C. SS-Teaching and Learning in the Design of Circuits and Integrated Systems I. 10:30-11:30 (Room María Fernández del Amo)

Session Chairs: Arancha Otín, Antonio José Ginés

Using JIGSAW-type Collaborative Learning for Integrating Foreign Students in Embedded System Engineering
Hector Posadas, Eugenio Villar and Fernando Herrera *(Universidad de Cantabria)*

Design and Development of an Anthropomorphic Robotic Arm for Educational Purposes
Javier Del Sol Rodriguez, Fernando Lopez-Colino, Guillermo Gonzalez de Rivera and Javier Garrido *(Universidad Autónoma de Madrid)*

A Freeware EDA Framework for Teaching Mixed-Mode Full-Custom VLSI Design
Jofre Pallarès, Francesc Vila, Stepan Sutula, Keith Sabine, Lluís Terés and Francisco Serra-Graells *(Centro Nacional de Microelectrónica)*

Session 2A. SS-Teaching and Learning in the Design of Circuits and Integrated Systems II. 12:00-13:20 (Room C)

Session Chairs: Mar Martínez, Lluis Terés

A first year, VHDL based, digital electronics course
José Daniel Muñoz Frías and Sadot Alexandres Fernández *(Universidad Pontificia Comillas)*

FFC NMR Relaxometers on Education - Topologies, control techniques and electromagnetic devices
António Roque, Duarte Sousa, Elmano Margato, Pedro Sebastião, Gil Marques and José Maia *(INESC-ID / IST)*

From Boolean Algebra to Processor Architecture and Assembly Programming in One Semester
José Matos, José Alves, Hélio Mendonça and António Araújo *(University of Porto)*

Promoting Student Autonomy in the Electronic Design Course
Maria Del Carmen Pérez Rubio, Álvaro Hernández Alonso and Raúl Mateos Gil *(Universidad de Alcalá de Henares)*

Session 2B. Low power / Low Voltage Analog Design. 12:00-13:20 (Room D)

Session Chairs: Eugenio García, Stelios Siskos

Front-end electronics for charged particle detection in 90 nm CMOS process
Rafael Lopez-Ahumada, Trinidad Sanchez-Rodriguez, Juan-Antonio Gomez-Galan, Manuel Sanchez Raya, Manuel Pedro Carrasco and Raul Jimenez *(Universidad de Huelva)*

0.13-µm CMOS Variable Gain Amplifier Using a Novel Tunable Triode Transconductor
Trinidad Sanchez, Juan-Antonio Gomez-Galan, Manuel Pedro, Antonio Lopez-Martin, Ramon Gonzalez Carvajal and Jaime Ramirez-Angulo *(Universidad de Huelva)*

High Performance Dual Supply Level Up/Down Shifter for a 0.6V – 1V Input/Output Range and 1.2V Output/Input
J. C. Garcia-Montesdeoca, Juan A. Montiel-Nelson, J. Sosa and Saeid Nooshabadi *(Universidad de las Palmas de Gran Canaria)*

Power Optimization and Stage Op-amp Linearity Relaxation in Pipeline ADCs with Digital Comparator Offset Calibration
Antonio Jose Gines, Eduardo Peralías, Cristina Aledo and Adoracion Rueda *(Instituto de Microelectrónica de Sevilla)*

Session 2C. FPGAs. 12:00-13:20 (Room María Fernández del Amo)

Session Chairs: Juan Carlos López, Emilio Olías

More Robustness and Flexibility for FPGA Based Networked Embedded Systems through Hardware Indirect Proxies
Jesús Barba, Fernando Rincón, Julio Dondo, David De La Fuente, Francisco Moya and Juan Carlos López *(Universidad de Castilla la Mancha)*

Collaborative Evolution Strategies on Evolvable Hardware Networked Elements
Francisco Javier Vazquez, Blanca Lopez, Juan Valverde, Eduardo De La Torre and Teresa Riesgo *(Universidad Politécnica de Madrid)*

Run-time adaptable FPGA-based embedded system for real-time hyperspectral unmixing

Julián Caba**, Teresa Cervero*, Julio Daniel Dondo**, Sebastián López**, Fernando Rincón**, Roberto Sarmiento* and Juan Carlos López**

(**Universidad de las Palmas de Gran Canaria)*

(***Universidad de Castilla la Mancha)*

FPGA Implemented Cut-Through vs Store-and-Forward Switches for Reliable Ethernet Networks
Armando Astarloa, Jesús Lázaro, Unai Bidarte, José Ángel Araujo and Naiara Moreira *(Universidad del País Vasco)*

Session 2D. Failure Analysis. 12:00-13:20 (Room Salón de Actos)

Session Chairs: Joan Figueras, Miquel Roca

Gate Oxide Breakdown Parameter Extraction with Ground and Power Supply Signature Measurements
Soonyoung Cha, Linda Milor and Woongrae Kim *(Georgia Institute of Technology)*

On the impact of supply voltage variation on the statistical reliability of a Spin-transfer-torque MRAM (STT-MRAM)
Elena Ioana Vatajelu, Rosa Rodriguez, Marco Indaco, Michel Renovell, Paolo Prinetto and Joan Figueras *(Universitat Politècnica de Catalunya)*

Automated exhaustive exploration of SET pulse propagation in nanometer ICs through CAD analysis
Salvador Barceló, Xavier Gili, Sebastia Bota and Jaume Segura *(Universitat Politècnica de Catalunya)*

Design Principles and Challenges for an Autonomous WSN for Structural Health Monitoring in Aircrafts
Markos Losada, Pablo Del Campo, Andoni Irizar, Pedro Ruiz and Apostolos Leventis *(Centro de Estudios e Investigaciones Técnicas)*

Session 3A. Image and Graphic Processing. 15:00-16:20 (Room C)

Session Chairs: Sebastián López, César Sanz

Implementation Tradeoffs of Triangle Traversal Algorithms for Graphics Processing
Pablo Royer, Pablo Ituero, Marisa López-Vallejo and Carlos A. López Barrio *(Universidad Politécnica de Madrid)*

An automatic tool for the static distribution of actors in RVC CAL based multicore designs
Miguel Chavarrias, Fernando Pescador, Eduardo Juarez and Matias J. Garrido *(Universidad Politécnica de Madrid)*

Efficient Implementation of Pattern Matching Recognition in Heterogeneus Architectures
Javier González-Bayón, Pablo Sánchez and Javier Barreda *(Universidad de Cantabria)*

Enhanced event-based stereo vision with Gabor filters
Luis Alejandro Camuñas-Mesa, Teresa Serrano-Gotarredona, Sio-Hoi Ieng, Ryad Benosman and Bernabé Linares-Barranco (*Instituto de Microelectronica de Sevilla - IMSE-CNM-CSIC*)

Session 3B. Analog Design. 15:00-16:20 (Room D)

Session Chairs: José M. de la Rosa, Pere Miribel

Highly-Linear Tunable Class AB CMOS Gm-C Filter with Automatic Tuning Control
Coro Garcia-Alberdi, Antonio Lopez-Martin (*Universidad Pública de Navarra*), Juan A. Galan (Universidad de Huelva), Jaime Ramirez-Angulo (*Klipsch School of Electrical and computer Engineering - New Mexico State University*), and Ramon G. Carvajal (Universidad de Sevilla)

Hierarchical Composition of Pareto-Optimal Fronts of Analog Circuits: Implementation Issues

Manuel Velasco-Jiménez, Rafael Castro-López, Elisenda Roca and Francisco V. Fernández (*Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC and Universidad de Sevilla*)

Bulk-Driven Three-stage Class-AB CMOS OTA

Elena Cabrera-Bernal (*Universidad de Sevilla*), Salvatore Pennisi and Alfio Dario Grasso (*University of Catania*)

Source Compensated Miller Op-Amps: A Simple Approach to Enhance Amplifier's Bandwidth
Jaime Ramírez-Angulo, Enrique Mirazo (*Klipsch School of Electrical and computer Engineering - New Mexico State University*), Javier Lemus, Alejandro Díaz-Sánchez (*INAOE*), Jose M. Algueta-Miguel, Antonio J. López-Martín (*Universidad Pública de Navarra*), and Ramón G. Carvajal (*Universidad de Sevilla*)

Session 3C. Integrated Sensors and Applications. 15:00-16:20 (Room María Fernández del Amo)

Session Chairs: Alkiviadis Hatzopoulos, Miguel Holgado

A Low-Power MOS-Only Potentiostatic Delta-Sigma ADC Architecture for Electrochemical Sensors
Jofre Pallarès, Stepan Sutula, Javier Gonzalo-Ruiz, Francesc Xavier Muñoz-Pascual, Lluís Terés and Francisco Serra-Graells *(Institut de Microelectrònica de Barcelona, Centro Nacional de Microelectrónic, IMB-CNM (CSIC), Spain)*

Development and Implementation of a Configurable Quadrant Photodetector
Roberto Esper-Chaín Falcón, Alfonso Medina Escuela and José Ramón Sendra Sendra (*Instituto Universitario de Microelectrónica Aplicada - Universidad de Las Palmas de Gran Canaria*)

Fully digital standard-cell based temperature sensor tolerant to supply voltage variability
Ivan de Paul, Carol de Benito, Sebastia Bota and Jaume Segura (*Electronics Systems Group, Universitat Illes Balears*)

Implementing a multisensory robotic platform for building collaborative monitored Robots
Julio Acosta (*ESPE extensión Latacunga, Universidad de las Fuerzas Armadas ESPE*), Guillermo González de Rivera and Javier Garrido (*Universidad Autónoma de Madrid*)

Session 3D. Reliability. 15:00-16:20 (Room Salón de Actos)

Session Chairs: Albert Comerma, Luís Entrena

System-Level Modeling of Microprocessor Reliability Degradation Due to TDDB

Chang-Chih Chen, Soonyoung Cha and Linda Milor *(School of Electrical and Comptuer Engineering, Georgia Institute of Technology, Atlanta)*

Modeling of Partially Cracked and Void Hole Defected Through Silicon Via Interconnections
Vasileios Gerakis, Alexandros Liolios and Alkis Hatzopoulos (*Aristotle University of Thessaloniki*)

Resistive Open Defect Characteritzation in 3D 6T SRAM memories
Raül Castillo, Daniel Arumi and Rosa Rodriguez-Montanes (*Departament d'Enginyeria Electrònica, Universitat Politècnica de Catalunya*)

Comparative of software-based hardening techniques for LEON 3 microprocessor
Luis Parra, Almudena Lindoso and Luis Entrena (*Microelectronics group, Electronic Technology Department, Universidad Carlos III de Madrid*)

Tutorial 1: Assessing and implementing the fault tolerance of digital circuits. 17:00-18:20 (Room C)

Dan Alexandrescu, Luca Sterpone and Celia López-Ongil

Iroc Technologies, Politecnico di Torino, Universidad Carlos III de Madrid

Traditionally, heavy ions radiation affecting digital systems working in avionics systems has been of huge interest. Nowadays, due to the shrinking technology process, Integrated Circuits became sensitive also to other kinds of radiation particles such as neutron that can exist at the earth surface and affects ground-level safety critical applications such as automotive or medical systems. The process of analyzing and hardening digital devices against soft errors implies rising the final cost due to time expensive fault injection campaigns and radiation tests, as well as reducing system performance due to the insertion of redundancy-based mitigation solutions. The main industrial problem arising is the localization of the critical elements in the circuit in order to apply optimal mitigation techniques. The proposal of this tutorial is to present and discuss different solutions currently available for assessing and implementing the fault tolerance of digital circuits, not only when the unique design description is provided but also at the component level, especially when Commercial-of-the-shelf (COTS) devices are selected.

Tutorial 2: Developing commercial IC designs projects from universities: a newcomer's guide. 17:00-18:20 (Room D)

Antonio López-Martín

Universidad Pública de Navarra

The design of industrial integrated circuits (IC) is a challenging task that involves several relevant issues often not considered by IC designers used to academic research projects. Issues such as time-to-market, manufacturing and non-recurring engineering (NRE) costs, design for test (DFT), manufacturability issues, yield, and intellectual property management, are highly relevant and often not considered in academic projects.

This 1-hour tutorial will provide an introduction to the area of industrial integrated circuit (IC) design, stressing these areas often not considered by IC designers in academia. Based on the experience of the author in research and development projects with companies such as

Azkoyen, Nacesa, Meggitt, Infineon and Seiko Epson, the tutorial tries to provide a step-by-step description of the way such projects are faced and developed. It covers both technical skills aimed to successfully develop an industrial IC design and management skills to negotiate budgets and intellectual property rights with the company.

Focus will be on practical aspects of industrial IC development and how to face it by a research group from an academic institution. A detailed case study of an ASIC developed by the author for contactless angular detection in automotive applications will serve to illustrate the design flow and different concepts treated in the talk.

Tutorial 3: Organic/Printed Electronics: Technology, Physical Design Kits and Basic Design Flows for new Plastic Electronics. 17:00-18:20 (Room María Fernández del Amo)

Jordi Carrabina, Lluís Terés

Universitat Autònoma de Barcelona, IMB-CNM (CSIC)

While silicon based technologies are evolving towards very advanced nanometric nodes less than 20□m., the emerging thin-flexible-organic-large-area electronics (printed electronics, PE), or even printed microelectronics (W/L □ 1 to 100 □m.) based on “plastic” substrates and functional inks are starting again the history of microelectronics at technology and device levels trying to grow up to application level by means of cell-libraries, design kits and the related EDA tools looking at the silicon path but far away from its costs and performances.

Performance and size of PE devices is far away from Si devices; nevertheless there are a lot of new applications which have been enabled by those new technologies where the rigid silicon/PCB electronics doesn’t have sense according to large area requirements (i.e. biosensors), low cost (i.e. tags) or flexibility (i.e. wearables). In the case that high performance is required the proposed solution is hybridization of “silicon on top of plastic” while keeping the overall system flexibility. From costs points of view Si foundries are several orders of magnitude more costly that PE houses, and thus device prototyping and production for small-medium series are also some orders of magnitude higher in silicon than in plastic. Additionally, while silicon foundries are being reduced in number and concentrated in a few poles all over the world, the PE technologies are expected to be greener than silicon ones and widespread (and specialized) potentially everywhere.

After reviewing the main printed-electronics technologies we will summarize the main characteristics, performances, cost factors and application domains for each one in order to keep clear the basic concepts around them.

Following the Si microelectronics experience we have proposed a methodology to go from early technology development stages up to physical design kit (PDK) and reusability based design flows by means of PCells based developments for basic technology structures, devices, std.-cells and inkjet gate-array (IGA) structures. Such a methodology has been applied to three different technologies and we will address the main results and conclusions.

Welcome Cocktail. 19:00-21:00

THURSDAY 27TH

Plenary Session 2. 9:00-10:00 (Room Salón de Actos)

Prof. Lukáš Sekanina, Brno University of Technology, Czech Republic

Lukas Sekanina received the MEng and PhD degree from the Brno University of Technology, Czech Republic, in 1999 and 2002. He is currently a full professor with the Faculty of Information Technology, Brno University of Technology. His research interests include evolutionary design and evolvable hardware. He received the Fulbright scholarship to work with NASA Jet Propulsion Laboratory in Pasadena in 2004. He was a visiting lecturer with Pennsylvania State University and a visiting researcher with University of Oslo in 2001. He has served as an associate editor of the IEEE Transactions of Evolutionary Computation, and editorial board member of Genetic Programming and Evolvable Machines journal, and International Journal of Innovative Computing and Applications. He coauthored over 150 papers mainly on evolvable hardware. He is a senior member of IEEE (Computational Intelligence Society).

From Evolvable Hardware to Approximate Computing

Abstract: Evolvable hardware is a technology which combines bio-inspired artificial intelligence with hardware design and reconfiguration. In this talk, I will survey recent development in the areas of evolutionary circuit design and FPGA-based evolvable systems. Several case studies will be presented to demonstrate strength and weakness of the evolutionary design method, including the combinational circuit synthesis and adaptive image filtering intended for FPGAs. The second part of the talk is devoted to approximate computing which is a modern design paradigm for energy-efficient computer-based systems. It exploits the fact that many applications are error resilient which means that their users are willing to accept less than perfect solutions, simply because the inaccuracies in the output are not recognizable, or they are well justified under some circumstances. The approximate circuit design problem can be formulated as a multi-objective optimization problem in which the accuracy and power consumption are conflicting design objectives. It will be shown how the principles of evolvable hardware can be utilized to approximate circuit designs.

Tutorial 4: How to Make Your Integrated Sensor Smarter. 10:00-11:20 (Room C)

Francesc Serra-Graells

IMB-CNM (CSIC)

More than Moore roadmaps predict a semiconductor market evolution towards new heterogeneous integrated system-on-chip products with built-in input and output transconductors. Unfortunately, it is not uncommon to find several examples of very promising sensors that could not fill the gap between sensor prototypes (devices) and final products (systems) due to the lack of suitable custom CMOS interfaces (circuits). This tutorial will introduce the design challenges associated with these read-out circuits, such as massive multi-

channel A/D conversion, sensor biasing control loops, tuning capabilities against technology deviations, and calibration strategies, as well as some other practical aspects related with the powering and packaging of full smart sensors. The low-power and compact area CMOS read-out integrated circuit (ROIC) proposals presented in this tutorial are taken from real smart sensors examples developed at IMB-CNM(CSIC) for applications such as fast clinical analysis, toxic gas classification, portable chemical sensing, infrared and X-ray imaging and remote powered sensing nodes.

Tutorial 5: Some ideas to thermal verification of FPGAs. 10:00-11:20 (Room D)

Eduardo Boemo

Universidad Autónoma de Madrid

Thermal verification of complex ICs can help the designer to detect if a particular block is working beyond specifications. A simple method is to extract the output frequencies of an array of ring-oscillators previously distributed in the die. The main advantage is that neither external transducers nor analog parts are necessary. Other possibility is to bias one of the clamping diodes usually present in the pads, and measure its junction forward voltage. In both cases, the measurement of temperature can be done in actual working conditions; that is, with the chip inside the case with its heat sink and fan. This tutorial explain main ideas to construct optimal sensors on FPGAs, calibration hints, and applications.

Tutorial 6: Digital on top implementation for mostly Analog designs. 10:00-11:20 (Room María Fernández del Amo)

Albert Comerma

Physikalisches Instiut – Heidelberg University

Mostly Analog designs present difficulties when some channels need to be assembled in a single die prototype. This normally leads to long sign-off times before submission of prototypes. This process can be accelerated taking the advantage on digital placement and routing tools.

The tutorial is focused on first identification of the cases where this design flow can be usable and profitable for the designer. Then it goes through the basic steps of the design flow to exemplify the process.

Session 4A. SS - Power management and ultra-low-power circuits. 12:00-13:20 (Room C)

Session Chairs: Eduard Alarcón, Marcelino B. Santos

Aging-Aware Dynamic Voltage or Frequency Scaling
Jorge Semião (*ISE – University of Algarve*), André Romão (*Silicongate*), Carlos Leong (*INESC-ID*), Marcelino Santos, Isabel Teixeira and Paulo Teixeira (*IST / INESC-ID*)

Efficiency Optimization of Multi-Mode Monolithic DC-DC Converters
Nuno Dias and Marcelino Santos (INESC-ID, Instituto Superior Técnico, Universidade de Lisboa)

An Output Capacitorless Low Dropout Voltage Regulator With A Novel Fast Settling Path
Jose Maria Hinojo, Clara Luján-Martinez, Antonio Torralba (*Universidad de Sevilla*), Jaime Ramirez Angulo (*Klipsch School of Electrical Engineering, New Mexico State University*), Guillermo Bistue (*Electronics and Communications Dept., CEIT and Tecnum, Universidad de Navarra)* and Javier Del Pino (*Institute for Applied Microelectronics IUMA (Universidad de Las Palmas de Gran Canaria)*

Self-Powered Adaptive Circuit Sampling for a Piezoelectric Harvester
Pere Miribel-Catala, Jordi Colomer-Farrarons, Jordi Lafuente Brinquis and Jaime López-Sánchez (*Electronics Department, Physics Faculty, Universitat de Barcelona, Discrete-2-Integrated Electronics, D2In Analog&MXS*)

Session 4B. Single Event Transient and Upset. 12:00-13:20 (Room D)

Session Chairs: Unai Alvarado, Celia López-Ongil

Assessing SET Sensitivity of a PLL
Marta Portela-Garcia, Celia Lopez-Ongil, Mario Garcia-Valderas and Luis Entrena (*Universidad Carlos III de Madrid*), Geert Thys and Steven Redant (*University of Leuven*)

Single Event Transients trigger instability in Sigma-Delta Modulators
Daniel Malagon (*Universitat de les Illes Balears*), Jose Manuel de La Rosa, Rocio Del Rio and Gildas Leger (*Instituto de Microelectronica de Sevilla - IMSE-CNM-CSIC*)

Latch SET capture in nanometer CMOS ICs: a detailed analysis
Xavier Gili, Salvador Barceló, Sebastià Bota and Jaume Segura (*Grupo de Sistemas Electrónicos de la Universitat de les Illes Balears*)

Fault Injection System for SEU Emulation in Zynq SoCs
Igor Villalta, Unai Bidarte, Gorka Santos, Asier Matallana and Jaime Jiménez (*Universidad del País Vasco/ Euskal Herriko Unibertsitatea UPV/EHU*)

Session 4C. Communications. 12:00-13:20 (Room María Fernández del Amo)

Session Chairs: Andoni Irizar, Eugeni Isern

A High Throughput Configurable Partially-Parallel Decoder Architecture for Quasi-Cyclic Low-Density Parity-Check Codes
Alaa Aldin Al Hariri, Fabrice Monteiro, Loïc Sieler and Abbas Dandache *(Université de Lorraine)*

CDMA PLC communications system
Dario Perez-Calderon, Vicente Baena Lecuyer, Jorge Chávez Orzáez, José García Doblado, Patricio López González, Ana Cinta Oria Oria *(Universidad de Sevilla)* and Eugenio Domínguez Amarillo *(Wind Inertia Technologies)*

Parallel Implementation of a Sample Rate Conversion and Pulse-Shaping Filter for High Speed Backhauling Networks
Aritz Alonso, Juan Francisco Sevillano and Igone Vélez *(Universidad de Navarra)*

Performance Evaluation of an AODV-Based Routing Protocol Implementation by Using a Novel In-Field WSN Diagnosis Tool

Gabriel Mujica, Rafael Zamacola, Jorge Portilla and Teresa Riesgo *(Universidad Politécnica de Madrid)*

Session 4D. Digital Design. 12:00-13:20 (Room Salón de Actos)

Session Chairs: Roberto Sarmiento, José Silva Matos

A Critical-Path Monitor for DVFS Systems without Datapath Replication
Hernán Cerqueira, Pablo Ituero and Marisa López-Vallejo *(Universidad Politécnica de Madrid)*

Defeating Microprobing Attacks using a Resource Efficient Detection Circuit
Michael Weiner *(Technische Universität München)*, Salvador Manich *(Universitat Politècnica de Catalunya)* and Georg Sigl *(Technische Universität München)*

Spiking neural networks signal processing
Josep Lluis Rosselló, Vicente Canals, Antoni Oliver, Antoni Morro and Miquel Alomar *(Universitat de les Illes Balears)*

Generation of Approximate Logic Circuits by Node Substitution
Antonio José Sánchez-Clemente, Luis Entrena and Mario García-Valderas *(Universidad Carlos III de Madrid)*

Session 5A. Organic electronics. 15:00-16:20 (Room C)

Session Chairs: Jordi Aguiló, Juan Montiel-Nelson

Top-down Design Flow for Application Specific Printed Electronics Circuits (ASPECs)
Manuel Llamas, Mohammad Mashayekhi, Jordi Carrabina *(Universitat Autònoma de Barcelona)*, Jofre Pallarès, Francesc Vila and Lluís Terés *(Consejo Superior de Investigaciones Científicas)*

Digital output MEMS pressure Sensor using Capacitance-to-Time Converter
Juan A. Montiel-Nelson, J. Sosa, R. Pulido *(Universidad de Las Palmas de Gran Canaria)*, A. Beriain, H. Solar and R. Berenguer *(Universidad de Navarra)*

Design of a monolithic CMOS-MEMS resonator as chaotic signal generator
Joan Barcelo, Jaume Segura, Sebastia Bota and Jaume Verd *(Universitat de les Illes Balears)*

Development of a Standard Cell Library and ASPEC design flow for organic Thin Film Transistor Technology
Mohammad Mashayekhi, Manuel Llamas, Jordi Carrabina *(Universitat Autònoma de Barcelona)*, Jofre Pallarès, Francesc Vila and Lluís Terés *(Consejo Superior de Investigaciones Científicas)*

Session 5B. Applications I. 15:00-16:20 (Room D)

Session Chairs: Ángel de Castro, Marta Portela

Path Length Comparison in Grid Maps of Planning Algorithms: HCTNav, A* and Dijkstra
Nafiseh Osati Eraghi, Fernando López-Colino, Angel de Castro and Javier Garrido *(Universidad Autónoma de Madrid)*

Environmental Wireless Sensor Network Deployment in Food Industry: from Theory to Practice

Elena Quesada, Mª Victoria Maigler, Alberto Barbado, Juan Valverde, Jorge Portilla and Teresa Riesgo *(Universidad Politécnica de Madrid)*

A high sensitivity and low power envelope detector for wireless sensor nodes
Dailos Ramos Valido, Hugo García Vázquez, Sunil Lalchand Khemchandani, Francisco Javier Del Pino Suárez *(Universidad de Las Palmas de Gran Canaria)*, Clara Luján Martínez *(Universidad de Sevilla)* and Guillermo Bistue García *(Universidad de Navarra)*

Design considerations of a small UAV platform carrying medium payloads
Juan Alberto Benito Carrasco, Guillermo González-De-Rivera, Javier Garrido *(Universidad Autónoma de Madrid)* and Roberto Ponticelli *(Robomotion)*

Session 5C. Architectures. 15:00-16:20 (Room María Fernández del Amo)

Session Chairs: Patrick Garda, Eugenio Villar

VIPPE, Parallel simulation and performance analysis of multi-core embedded systems on multi-core platforms
Luis Díaz, Eduardo Gonzalez, Eugenio Villar and Pablo Sanchez *(Universidad de Cantabria)*

Energy-based Fair Queuing Scheduling Implementation for Battery-limited Mobile Systems
Jianguo Wei, Rong Ren, Eduardo Juarez and Fernando Pescador *(Universidad Politécnica de Madrid)*

Multithreading Parallel Bit Plane Coding
Imen Mhedhbi, Khalil Hachicha and Patrick Garda *(University Pierre and Marie Curie)*

Automatic deployment of component-based embedded systems from UML/MARTE models using MCAPI
Alejandro Nicolás, Hector Posadas, Pablo Peñil and Eugenio Villar *(Universidad de Cantabria)*

Session 5D. Device Technology. 15:00-16:20 (Room Salón de Actos)

Session Chairs: Serge Bernard, Linda Milor

CMOS Continuous-Time Selective Change Driven Vision Sensor
Fernando Pardo, Jose A. Boluda and Francisco Vegara *(Universitat de València)*

Characterization of a Prototype FG MOSFET Dosimeter for X-Ray Radiotherapy
Miquel Roca, Eugeni Isern, Eugeni García-Moreno *(Universitat de les Illes Balears)*, Joan Font-Gelabert *(Hospital Universitari Son Espases)*, Joan Cesari and Alvaro Pineda *(iC-Málaga)*

Design of an implantable nano-enabled biomedical device for in-vivo glucose monitoring
Esteve Juanola-Feliu, Pere Lluís Miribel-Català, Cristina Páez-Avilés, Jordi Colomer-Farrarons, Manel González-Piñero and Josep Samitier Martí *(Universidad de Barcelona)*

Compact cryptoprocessor for securing wireless communications in FECG portable instrumentation
Luis Parrilla, Encarnacion Castillo, Diego Pedro Morales, Antonio García *(Universidad de Granada)*, Francisca Sonia Molina and Jesús Florido *(Hospital Clínico Universitario San Cecilio)*

Panel: Quo Vadis Zero Power Design: A System-Driven Debate. 16:20-18:00 (Room Salón de Actos)

Challenge: Address compromise conflicting requirements to concurrently trade-off between low power/system performance/reliability and other metrics.

Eduard Alarcón (UPC)
Linda Milor (Georgia Tech)
Marcelino Santos (SiliconGate/INESC/IST)
Stelios Siskos (Aristotle University of Thesaloniki)
Eugenio Villar (Univ. Cantabria)
Alex Yakovlev (Univ. NewCastle)
Antonio Rubio, CS, (UPC)

Embedded Tutorial (Tutorial 7)

Energy harvesting: device, circuit and system co-design and on-chip integration

Eduard Alarcón

Universitat Politècnica de Catalunya

The concept of harvesting ambient energy as an alternative power source for supplying integrated circuits aiming more miniaturized and distributed applications has been gaining momentum in the past years. A functional energy harvesting system, both in terms of available power and compatibility with system integration, requires concurrently addressing the energy transducing devices together with power management circuits. This talk will address the topic of power management circuits specific for harvesters, particularly emphasizing tight joint characterization, modeling and circuit co-design of the energy transducing devices and the power management frontend integrated circuits.

Social Event and Conference Dinner. 18:30-23:00

FRIDAY 28TH

Session 6A. Applications II. 9:40-11:00 (Room C)

Session Chairs: Roc Berenguer, Carlos López-Barrio

An integrated DC-AC inverter for electroluminescent lamps
Ioannis Sidiropoulos and Stylianos Siskos *(Aristotle University of Thessaloniki)*

A Varying Density 3D Laser Scanner for Unmanned Ground Vehicles Mapping and Obstacle Detection
José Ignacio Rejas Hernán, Manuel Prieto Perez-Borroto, Alberto Sanchez Gonzalez, Guillermo Glez-De-Rivera Peces and Javier Garrido Salas *(Universidad Autónoma de Madrid)*

Setup of a communication and control systems of a quadrotor type Unmanned Aerial Vehicle
Guadalupe Crespo, Guillermo González de Rivera, Javier Garrido *(Universidad Autónoma de Madrid)* and Roberto Ponticelli *(Robomotion)*

Low Frequency PWM Modulation for High Efficiency Class-D Audio Driving
Tiago Domingues, Marcelino Santos and Gonçalo Tavares *(INESC-ID / IST)*

Session 6B. Modeling. 9:40-11:00 (Room D)

Session Chairs: Rosa Rodríguez Montañés

Substrate Coupling Modeling in Integrated Circuits using Analytical Green's Function
Saiyd Ahyoune, Javier José Sieiro Cordoba, José Maria Lopez-Villegas and Maria Nieves Vidal Martinez *(Universitat de Barcelona)*

An Efficient Behavioral Description Frontend Tool for Mixed-Mode SPICE Simulation
Alvaro Gomez-Pau, Luz Balado, Joan Figueras *(Universitat Politècnica de Catalunya)* and Abhijit Chatterjee *(Georgia Tech)*

Analysis of Substrate Noise Coupling for Frequencies up to 100GHz
Vasileios Gerakis, Christos Fontounasios and Alkis Hatzopoulos *(Aristotle University of Thessaloniki)*

Design criteria for a discrete time chaos based true random number generator
José Luis Valtierra Sánchez de La Vega and Ángel Rodríguez Vázquez *(INAOE)*

Session 6C. Digital Signal Processing. 9:40-11:00 (Room María Fernández del Amo)

Session Chairs: Eduardo Juárez, Pablo Sánchez

Hardware Implementation of an Efficient Correlator from Golay Pairs Derived from Kernels of Lengths 2, 10 and 26
María Del Carmen Pérez Rubio, Enrique García Nuñez, Álvaro Hernández Alonso, Jesús Ureña Ureña, Juan Jesús García García, J. María Castilla Gómez and Alejandro Lindo Mañas *(Universidad de Alcalá)*

Angle Localization and Orientation System with 4 receivers and based on Audible Sound Signals

Santiago Elvira, Angel de Castro, Guillermo Glez-De-Rivera and Javier Garrido *(Universidad Autónoma de Madrid)*

Optimization of non-uniform grid projection image super-resolution algorithms by reduced granularity and modified addressing
Tomasz Szydzik *, Eduardo Quevedo**, Gustavo Marrero Callico*, Antonio Núñez Ordóñez*, Felix Tobajas* and Roberto Sarmiento*

*(*Universidad de las Palmas de Gran canaria)*

*(**Plataforma Oceánica de Canarias)*

On the Efficiency of Comb Structures for Sigma-Delta ADCs
Gerardo Molina Salgado, Gordana Jovanovic Dolecek *(INAOE)* and Jose de La Rosa *(Instituto de Microelectrónica de Sevilla)*

Session 7A. Analog III. 11:40-13:00 (Room C)

Session Chairs: José M. López Villegas, Antonio Torralba

Full passive RFID pressure sensor with a low power and low voltage time to digital interface
Andoni Beriain, Ainara Jimenez-Irastorza, Roc Berenguer *(Universidad de Navarra)*, Juan A. Montiel-Nelson, Javier Sosa and Ruben Pulido *(Universidad de Las Palmas de Gran Canaria)*

A power sensing circuit for solar cells MPP tracking
Theodoros Papaioannou, Ioannis Kosmadakis and Stylianos Siskos *(Aristotle University of Thessaloniki)*

A Low Power CMOS Temperature-to-Frequency Converter for RFID applications
Guillermo Bistue, Hector Solar, Erik Fernandez, Clara Lujan-Martinez *(Universidad de Sevilla)*, Javier Del Pino and Unai Alvarado *(CEIT)*

Spatial Detection System for Mini-Secondary Electrons Detectors
Alejandro Garzón-Camacho, Begoña Fernández, Marcos A. Alvarez, Joaquín Ceballos and Jose M. De La Rosa *(Instituto de Microelectrónica de Sevilla)*

Session 7B. Biomedical Electronics. 11:40-13:00 (Room D)

Session Chairs: Jordi Carrabina

A portable point-of-use EIS device for in-vivo biomedical applications
Jaime Punter *(Universitat de Barcelona)*

Simple and Efficient Removal of Baseline Drift in Electrocardiographic Signal Acquisition
Antonio Lopez-Martin, Maria Espadas Sucunza, Alejandra Arribas Bartolomé, Jaime Ramirez-Angulo and Ramon G. Carvajal *(Universidad Pública de Navarra)*

Characterization of electrode-skin impedance of textile electrodes
Cristina C. Oliveira, José Machado Da Silva, Antonio J. Salazar, Ruben Dias and Bruno Mendes *(INESC TEC, FEUP)*

A MEMS Design Tool for Blood-Pressure Sensing
Jose Ángel Miguel Díaz, Yolanda Lechuga and Mar Martinez *(Universidad de Cantabria)*

Session 7C. Built-In Self-Test. 11:40-13:00 (Room María Fernández del Amo)

Session Chairs: Luz Balado, Michel Renovell

A Microprogrammed Control Path Architecture for an Embedded IEEE 1149.1 Test Coprocessor
Ukbagiorgis I Gebremeskel and José M. M. Ferreira *(Buskerud and Vestfold University College)*

ADC Built-in-Self-Test Based on a Pseudorandom Uniform Noise Generator
Guiomar Evans *(Faculdade de Ciências da Universidade de Lisboa)*

Memory BIST for On-Chip Monitoring of Resistive-Open Defects due to Electromigration and Stress-Induced Voiding in an SRAM Array
Woongrae Kim, Soonyoung Cha and Linda Milor *(Georgia Institute of Technology)*

Conference Closing Session. 13:00-13:30 (Room Salón de Actos)